LEAKAGE TEST

109

DEVICE

(DUT)

PRE-CHARGE DEVICE

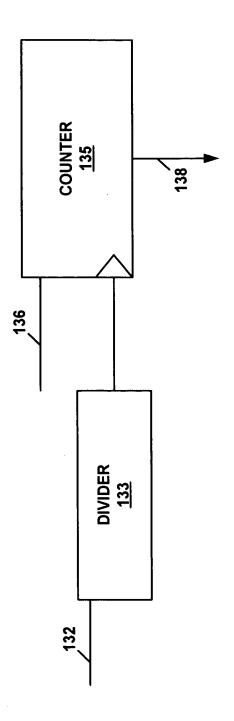
20

160

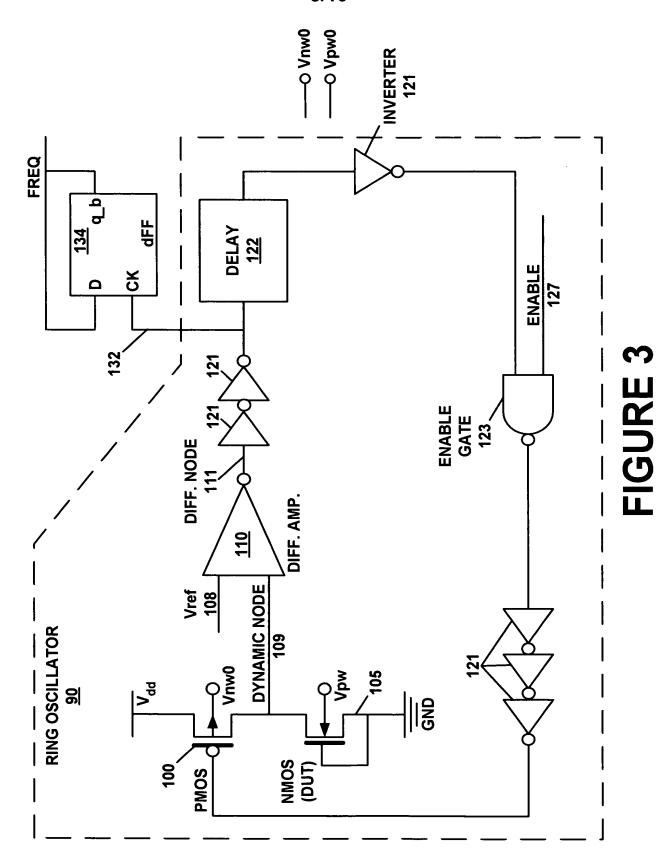
FIGURE 1

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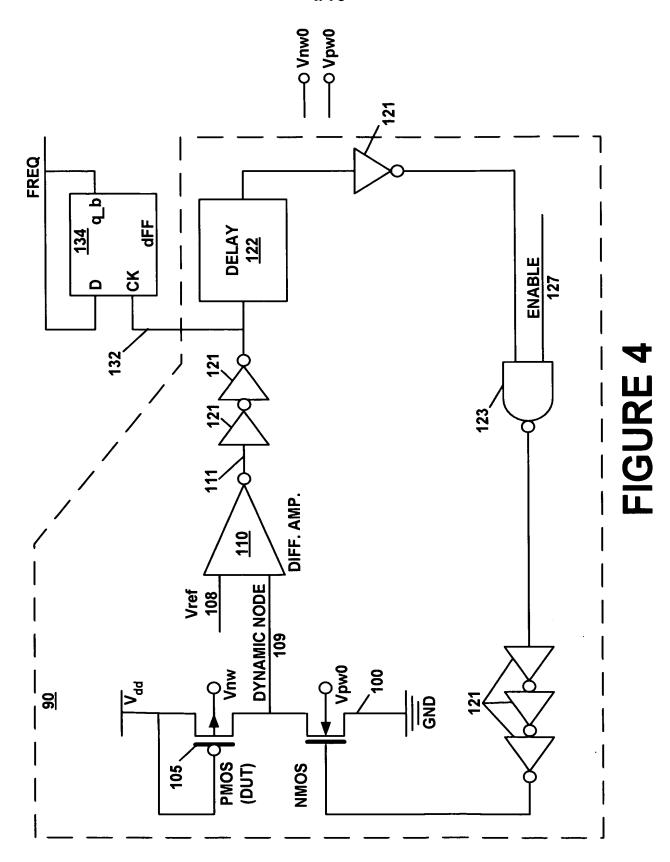
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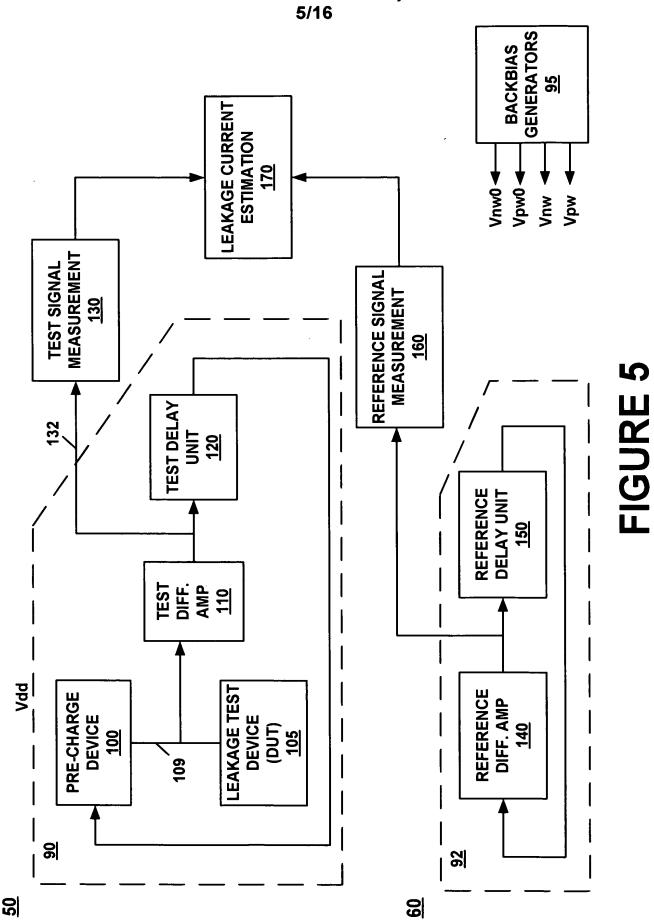




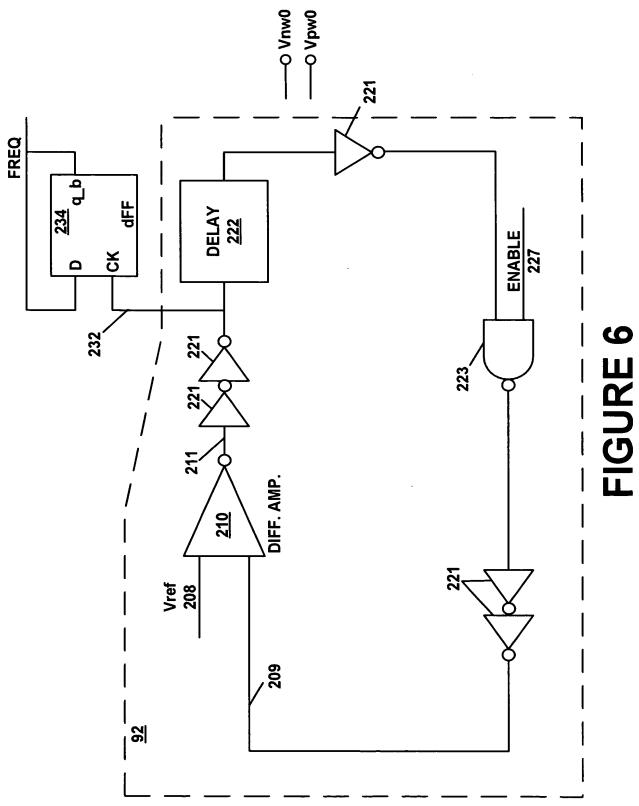






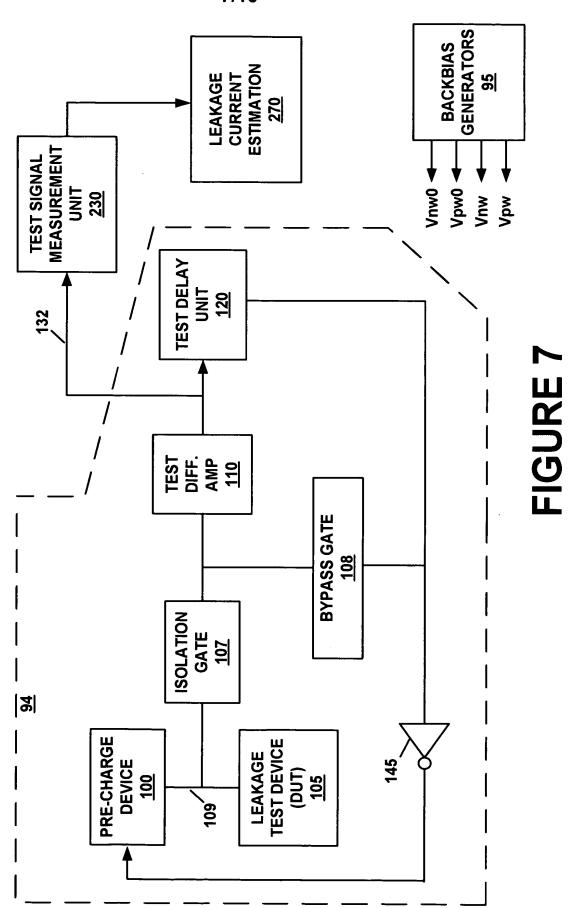






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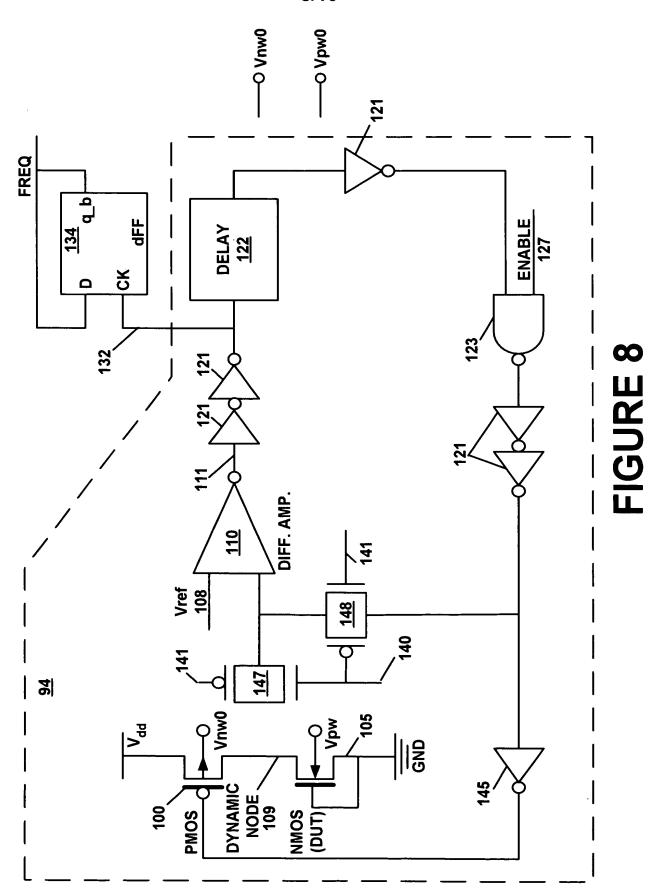
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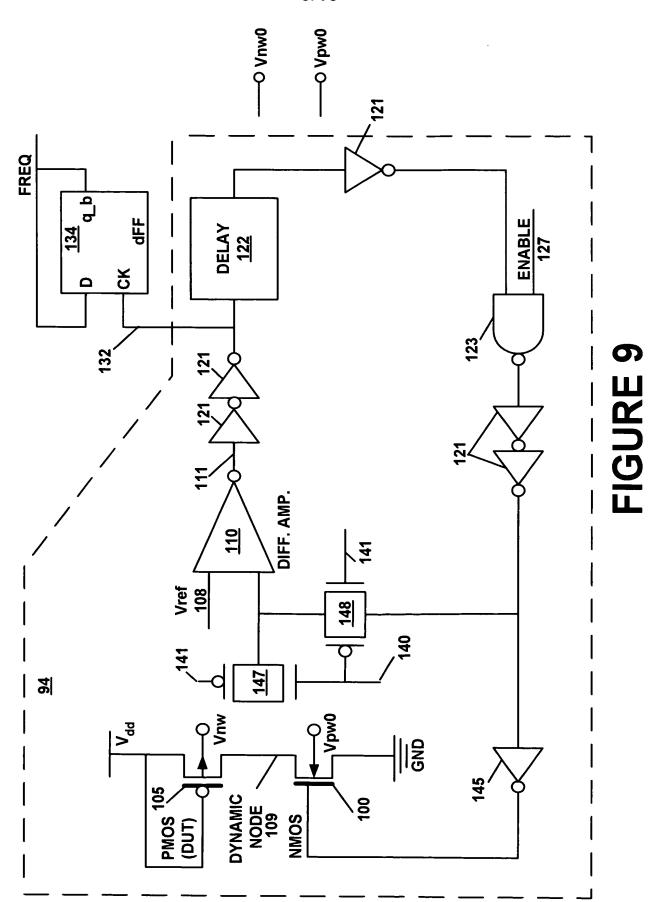
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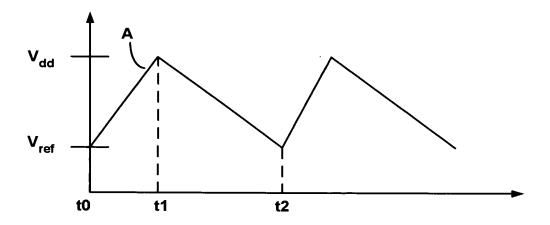


FIGURE 10A

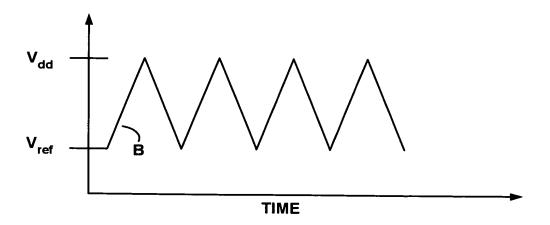


FIGURE 10B

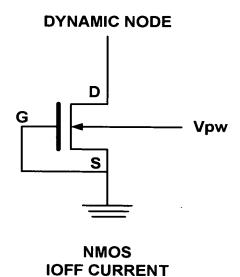
TITLE: SYSTEM AND METHOD FOR MEASURING TRANSISTOR LEAKAGE CURRENT WITH A RING OSCILLATOR WITH BACKBIAS CONTROLS

Inventor (s): Shingo Suzuki

Attorney Docket #: TRAN-P140.CIP

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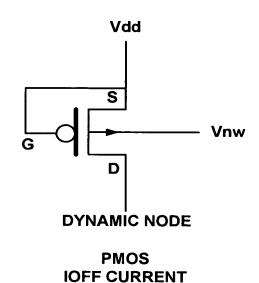
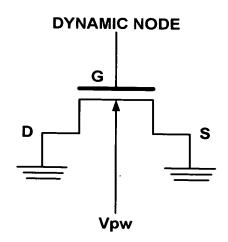


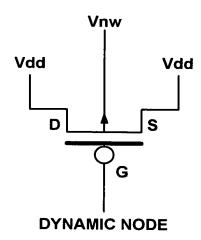
FIGURE 11

FIGURE 12

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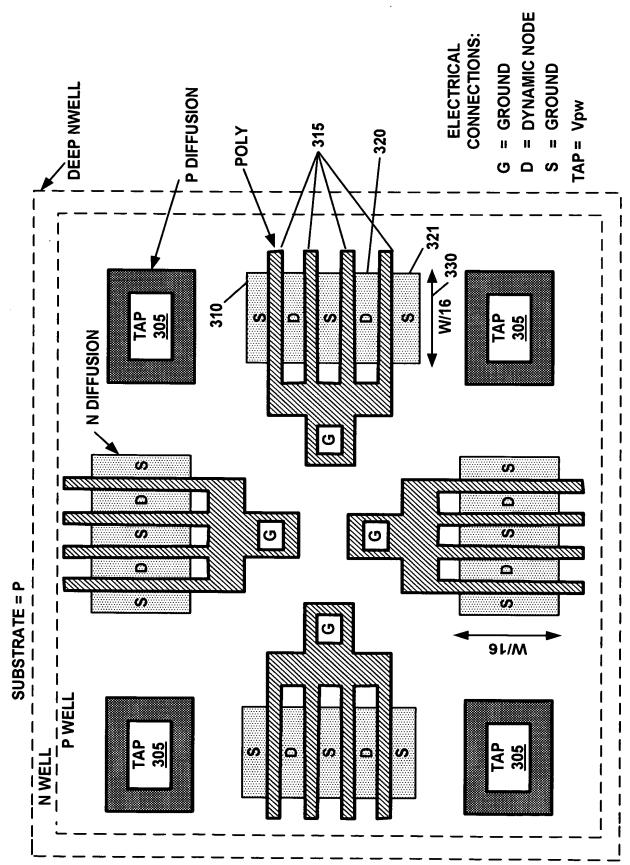
PMOS GATE LEAKAGE CURRENT

NMOS GATE LEAKAGE CURRENT

FIGURE 13

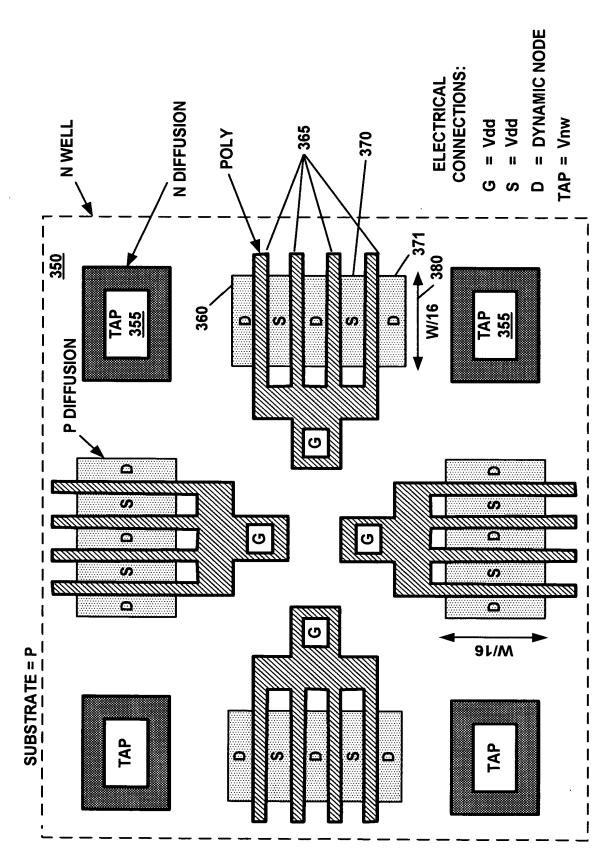
Attorney Docket #: TRAN-P140.CIP

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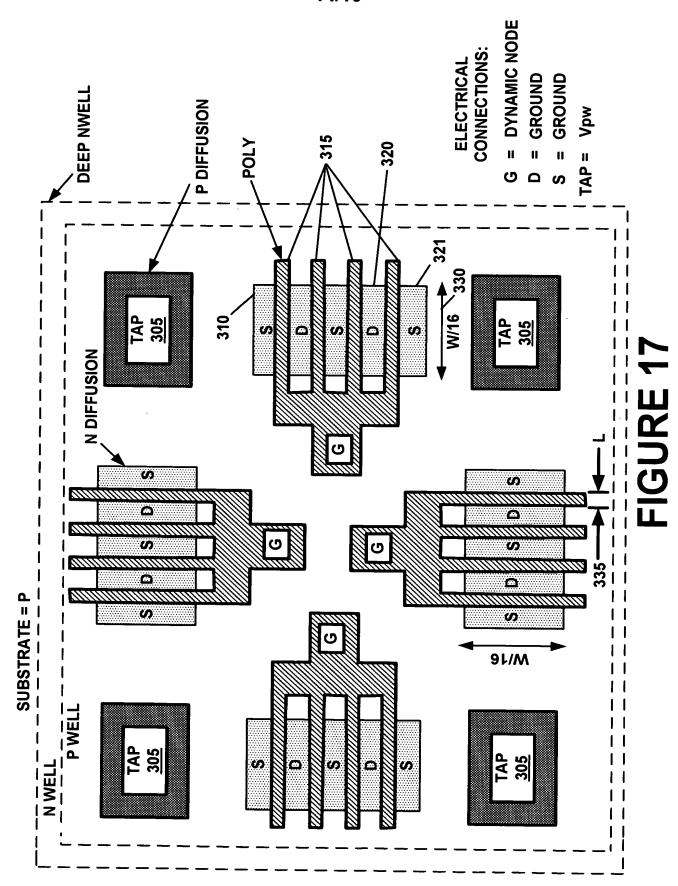
Attorney Docket #: TRAN-P140.CIP

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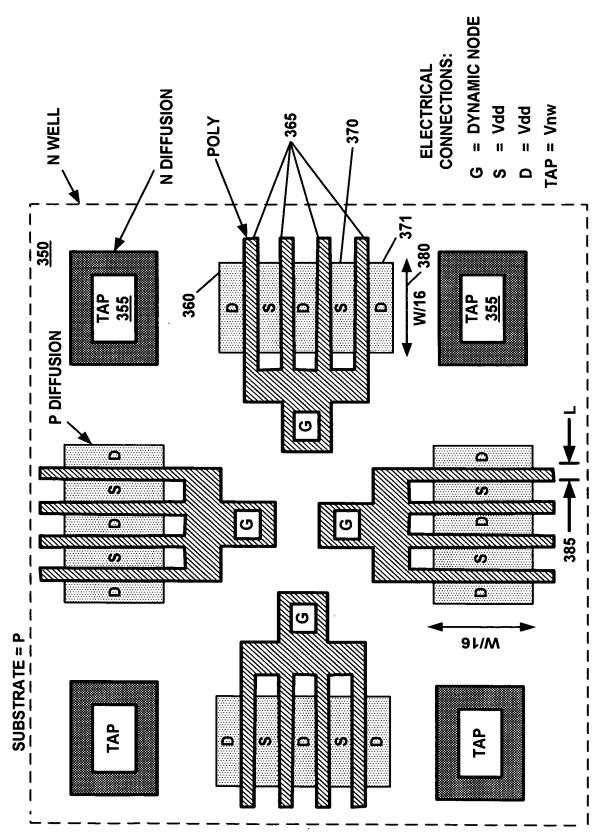
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